REMARKS

Attached herewith is a petition and fee for a one-month time extension.

Claims 1, 3, 5-7, 9, and 11-20 are all the claims presently pending in the application. Claims 2, 4, 8, and 10 are canceled.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner objects to the drawings for allegedly failing to show the clock-based description discussed in the specification.

Claims 1, 3, 5-7, 9, and 11-20 stand rejected under 35 USC §112, second paragraph, as allegedly being indefinite and for allegedly omitting essential structural connections.

Applicants gratefully acknowledge the Examiner's indication that there is allowable subject matter, since the prior art currently of record fails to reasonably suggest the techniques disclosed in the present invention.

The above rejections are discussed hereinbelow, in view of the above claim amendments.

I. THE CLAIMED INVENTION

As described and as defined in, for example, claim 1, the claimed invention is directed to an apparatus for estimating power consumption. A behavioral synthesis unit to which an algorithm-level description is input converts the algorithm-level description to a clock-based description and behavioral synthesis information. A clock-based simulation unit to which the clock-based description and behavioral synthesis information are input executes a clock-based simulation and calculates a power consumption factor by tracing the state of a variable in the clock-based description. The power consumption factor of a storage element is calculated by determining whether an array variable in the clock-based description is mapped to a memory or to registers, using the behavior synthesis information.

Conventional methods, as described beginning at line 12 on page 1, can be broken down into either an RTL HDL simulation (down to the gate level) or a clock-based simulation. As explained at lines 1-3 on page 3, the clock-based description has a lower level

of abstraction than the algorithmic language and a higher level of abstraction than the RTL HDL. As stated at lines 6-8 of page 10, the RTL HDL simulation is much slower than clock-based simulation, thereby allowing the present inventors to recognize that perhaps the benefits of both basic methods can be somehow combined relative to calculating power consumption estimations.

Therefore, in contrast to the conventional method, the present invention uses the clock-based simulation because of its inherent speed. Then, as the behavioral synthesis information is available, the specific form of storage developed by the behavioral synthesis process can be determined (e.g., whether a storage unit ended up being a memory or a register or register bank), thereby allowing the power consumption factor to be precisely calculated for the resultant type of storage. Therefore, the present invention retains both the speed of the clock-based simulation and the accuracy of conventionally slower simulations.

II. THE DRAWING OBJECTION

The Examiner objects to the drawings for allegedly failing to show the clock-based description discussed in the specification, including, even more particularly, Figures 9A, 9B, and 9C, for allegedly failing to be "... useful in describing setting of toggle rate and transition probability of an array", as described on page 6 of the specification.

In response, Applicants submit that the discussion in any specification is directed to one having ordinary skill in the art and that details presumed to be known in that art are not described in detail simply because they are presumed to be understood in the art.

In the present application, as described in the discussion in the BACKGROUND section beginning on page 1, the art of the present invention is that of simulation of circuits, including simulation/calculation of power consumption. Therefore, the instant specification presumes that the reader understands concepts in this art.

However, Applicants believe that the instant specification actually does explain these concepts even if this presumption of knowledge is not satisfied in the reader, as explained shortly.

As best understood, the Examiner's confusion is actually focused on two specific points: (1) the clock-based description of the specification; and, (2) the impact of Figures 9A-9C relative to "describing setting of toggle rate and transition probability of an array".

The description in the specification for these Figs. 9A-9C has been amended above to be consistent with the description at lines 21-25 of page 14, which specification amendment is believed to address the Examiner's concern about the description of these figures.

Returning now to the clock-based simulation technique, this technique is described beginning at line 15 on page 2 (i.e., paragraph [0005]), wherein is described that Japanese patent publication JP-P2001-109788A discusses this simulation technique. A copy of this Japanese patent publication was submitted via IDS with the original filing of the instant application.

In order for the Examiner to better understand the description of this method in the present application, a machine translation of JP-P2001-109788A is attached to this Amendment. It is noted that the "equations" themselves do not show up in this machine translation. However, these missing "equations" are software modules written in common computer instructions that are readable in the original IDS-supplied Japanese publication JP-P2001-109788A, since these code sections appear in the "English" of common software language instructions.

Thus, the instant specification is written presuming that the reader is familiar with the technique in JP-P2001-109788A, and one feature of the technique of the present invention is that this clock-based simulation technique can be used specifically for determination of power consumption estimates for memory units in a circuit design and that the type of storage element can later be determined by consulting the behavioral synthesis information (e.g., whether the storage element is based on an architecture of registers or is based upon an architecture of a memory unit) once this synthesis phase has processed to the point that the storage elements have been designed. The clock-based simulation technique treats all memory functions in that simulation as an array-variable, thereby allowing this simulation to calculate factors of power consumption such as toggle rate and transition probability.

However, Applicants believe that this technique is sufficiently described in the present application even without any resort to this earlier Japanese publication.

That is, the description at line 17 of page 9 through line 4 of page 10 clearly describes how the toggle rate and transition probability are calculated in the clock-based simulation. This discussion is subsequently related to Figure 8. Thus, Applicants submit that one having ordinary skill in the art would indeed be able to understand clock-based simulation even from the brief discussion in the present application, at least to the extent necessary to understand the present invention and realizing that the present invention is not intended to teach the details of the clock-based simulation, since it is presumed to be a software module available to perform its normal simulation role in implementing the present invention.

Therefore, Applicants respectfully request that the Examiner reconsider and withdraw this objection.

III. THE 35 USC § 112, SECOND PARAGRAPH REJECTIONS

Claims 1, 3, 5-7, 9, and 11-20 stand rejected under 35 USC §112, second paragraph, as allegedly being indefinite and for allegedly omitting essential structural connections.

Applicants believe that the above claim amendments address the concerns of the Examiner, as best understood.

Therefore, the Examiner is respectfully requested to reconsider and withdraw these rejections.

IV. FORMAL MATTERS AND CONCLUSION

The Examiner objected to the title as being non-descriptive. Applicants believe that the title amendment appropriately addresses the Examiner's concerns and respectfully requests that the Examiner reconsider and withdraw this objection.

In view of the foregoing, Applicant submits that claims 1, 3, 5-7, 9, and 11-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 11/27/06

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